

What is claimed is:

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4 the underlying conductive material (e.g., 3, 5) and the at least one third opening (e.g., 18,  
5 20) is filled with conductive material to form a contact or a via (e.g., 23, 25).

1                   8. The process of claim 1, wherein the step of etching the exposed  
2 dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a  
3 quadrilateral cross-section.

1                   9. The process of claim 1, wherein the step of etching the exposed  
2 dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a  
3 square cross-section.

1                   10. The process of claim 1, wherein the step of etching the exposed  
2 dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has substantially a  
3 rectangular cross-section.

1                   11. The process of claim 1, wherein the step of etching the exposed  
2 dielectric (e.g., 1) forms at least one third opening (e.g., 18, 20) that has a feature size of  
3 about 0.5 micron or less.

1                   12. The process of claim 1, wherein substantially no etch stop layer is  
2 deposited at the bottom of the trench.

1                   13. A process for manufacturing an integrated circuit, the process  
2 comprising:

3                   providing a substrate comprising silicon dioxide dielectric layer (e.g., 1)  
4 over a conductive material;

5                   depositing a silicon nitride hardmask (e.g., 7) over the dielectric layer;

6                   applying a first photoresist (e.g., 9) over the hardmask and photodefining at  
7 least one elongated opening;

8                   etching the hardmask and partially etching the dielectric to deepen the at  
9 least one elongated opening (e.g., 11) to form at least one trench (e.g., 13), the trench  
10 forming a bottom in the dielectric layer (e.g., 1);

11                  stripping the first photoresist (e.g., 9);

12                  applying a second photoresist (e.g., 15) and photodefining at least one  
13 second elongated opening (e.g., 17, 19) across the at least one trench;

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14                   selectively etching the dielectric (e.g., 1) from the bottom of the trench  
15 (e.g., 13) down to the underlying conductive material (e.g., 3, 5); and  
16                   removing the second photoresist (e.g., 15) and the hardmask (e.g., 7).

1                   14. A method of making an integrated circuit comprising defining a via or  
2 contact (e.g., 23, 25) by the intersection of a first elongated opening (e.g., 11) in a first  
3 mask (e.g., 9) and a second (e.g., 17, 19) elongated opening in a second mask (e.g., 15),  
4 and using at least one of the mask openings to define the location of a conductor (e.g., 3,  
5) to which the via or contact (e.g., 23, 25) is to be connected.

1                   15. An integrated circuit, comprising at least one connection (e.g., 23, 25),  
2 wherein the at least one connection has substantially a quadrilateral cross-section, wherein  
3 the quadrilateral has a feature size of about 0.5 micron or less.

1                   16. The integrated circuit of claim 15, further comprising at least one  
2 trench having a bottom (e.g., 13), wherein there is substantially no etch stop layer at the  
3 bottom of the trench.

1                   17. The integrated circuit of claim 15, wherein the at least one connection  
2 (e.g., 23, 25) has substantially a square cross-section.

1                   18. The integrated circuit of claim 15, wherein the at least one connection  
2 (e.g., 23, 25) has substantially a rectangular cross-section.

1                   19. The integrated circuit of claim 15, wherein the at least one connection  
2 (e.g., 23, 25) is a contact or a via.

1                   20. The integrated circuit of claim 15, wherein the quadrilateral has a  
2 feature size of about 0.25 micron or less.

1                   21. An integrated circuit, comprising at least one connection (e.g., 23, 25),  
2 wherein the at least one connection has substantially a quadrilateral cross-section, wherein  
3 the quadrilateral has a feature size of about 0.18 to about 0.14 micron.

1                   22. The integrated circuit of claim 21, wherein the quadrilateral has a  
2 feature size of about 0.18 to about 0.16 micron.

1                   23. An integrated circuit, comprising a connection, wherein the connection  
2 (e.g., 23, 25) has substantially a quadrilateral cross-section, wherein the quadrilateral has a  
3 feature size of about 0.12 micron.

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